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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,158	04/09/2004	Vamsi Boppana	162.8030USU	1180

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EXAMINER	
PARIHAR, SUCHIN	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/822,158	BOPPANA ET AL.	
	Examiner	Art Unit	
	Suchin Parihar	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *09 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-9,11-20,22-25 and 27-32* is/are rejected.

7)☒ Claim(s) *5,10,21 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to application 10/822,158, filed on 4/9/2004. Claims 1-32 are pending in this application.

Claim Objections

1. Claim 24 is objected to because of the following informalities: Claim 24 begins "The storage medium of claim 16"; examiner suggests amending claim 24 to the following –The storage medium of claim 17--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. **Claims 11 and 27 are rejected under 35 U.S.C. 112, second paragraph**, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. With respect to claims 11 and 27, both claims recite "regression analysis estimation". However, this specification fails to describe how "regression analysis estimation" provides a diffusion region width w.

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. **Claims 12-14 and 28-30 are rejected under 35 U.S.C. 112, first paragraph**, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in

the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Examiner notes that the specification refers to the importance of MTS in obtaining an accurate estimate of wiring capacitance. However, the specification fails to enable one with ordinary skill in the art to utilize MTS to obtain an accurate estimate of wiring capacitance. Specifically, how does one go about using MTS(t), which is shown as part of the equation in claims 12 and 28. In addition, the significance of the absolute value |MTS(t)| is not supported in the specification.

6. **Claims 4 and 20 are rejected under 35 U.S.C. 112, first paragraph**, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. With respect to claims 4 and 20, the specification fails to explicitly describe the use of 5% regarding the accuracy of statistical pre-layout estimation of standard cell.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. **Claims 1, 2, 8, 9, 16-18, 24, 25 and 32 are rejected under 35 U.S.C. 102(b)** as being anticipated by Gupta (6,163,877).

9. With respect to claims 1 and 17, Gupta teaches: receiving a pre-layout representation of said standard cell (Col 6, lines 60-68, i.e. receiving schematic diagram or netlist prior to layout); applying at least on transformation to said pre-layout representation to obtain an estimated representation (Col 7, lines 32-40, i.e. discussion of folding transistors to satisfy performance constraints); and characterizing said estimated representation to obtain said pre-layout estimation of said characteristic of said standard cell (Col 2, lines 1-10, i.e. discussion of Figure 3, layout representation before and after transistor fold takes place).

10. With respect to claims 2 and 18, Gupta teaches all the elements of claims 1 and 17, from which the claims depend respectively. Gupta teaches: wherein said pre-layout representation is selected from the group consisting of: a spice netlist, a BDD-based transistor structure representation, and a pre-layout structural representation (Col 6, lines 60-68, i.e. discussion of circuit description being a schematic diagram [structural representation] or a net list).

11. With respect to claims 8 and 24, Gupta teaches all the elements of claims 1 and 17, from which the claims depend respectively. Gupta teaches: wherein said at least one transformation is selected from the group consisting of: transistor folding, diffusion area and perimeter assigning of transistors of said standard cell transformation, and adding wiring capacitances to said pre-layout representation (Col 7, lines 32-40, i.e. discussion of folding transistors to satisfy performance constraints).

12. With respect to claims 9 and 25, Gupta teaches all the elements of claims 8 and 24, from which the claims depend respectively. Gupta teaches: wherein said transistor

folding transformation is performed prior to said diffusion area and perimeter assigning of transistors of said standard cell transformation, and adding wiring capacitances to said pre-layout representation (Col 3, lines 54-67, i.e. discussion of considering transistor folding before placement).

13. With respect to claims 16 and 32, Gupta teaches all the elements of claims 1 and 17, from which the claims depend respectively. Gupta teaches: wherein said characteristic is selected from the group consisting of: a cell footprint and a pin placement of said cell (Col 6, lines 45-60, i.e. discussion of different cell orientations of transistor cells in the layout, orientations which would modify the placement of cell footprints within the layout).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. **Claims 3, 6, 7, 15, 19, 22, 23 and 31 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Gupta (6,163,877) in view of Teene (6,272,668).

16. With respect to claims 3 and 19, Gupta teaches all the elements of claims 1 and 17, from which the claims depend respectively. Gupta does not teach: wherein a statistical pre-layout estimator is used to obtain said pre-layout estimation of said

standard cell. However, Teene teaches: wherein a statistical pre-layout estimator is used to obtain said pre-layout estimation of said standard cell (Col 8, lines 65-67, i.e. element 292 performs optional static timing analysis with pre-layout estimated timings). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Teene into the invention of Gupta because Teene suggests that this pre-layout timing analysis can improve the invention of Gupta by quickly revealing gross timing violations, critical paths, for both worst-case and best-case conditions, plus the effect of estimated power dissipation (see Col 8 line 65 - Col 9 line 4), all of which are critical elements well known in the art of circuit design.

17. With respect to claims 6 and 22, Gupta teaches all the elements of claims 1 and 17, from which the claims depend respectively. Gupta does not teach: wherein said characteristic comprises a parasitic-dependent standard cell characteristic. However, Teene teaches: wherein said characteristic comprises a parasitic-dependent standard cell characteristic (Col 10, lines 30-38, i.e. discussion of pre-layout timing/capacitance values of the standard cell component). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Teene into the invention of Gupta because Teene suggests that this pre-layout timing analysis can improve the invention of Gupta by quickly revealing gross timing violations, critical paths, for both worst-case and best-case conditions, plus the effect of estimated power dissipation (see Col 8 line 65 - Col 9 line 4), all of which are critical elements well known in the art of circuit design.

18. With respect to claims 7 and 23, Gupta in view of Teene teaches all the elements of claims 6 and 22, from which the claims depend respectively. Gupta does not teach: wherein said parasitic-dependent standard cell characteristic is selected from the group of standard cell characteristics consisting of: timing, power, input capacitance, noise, and any other parasitic-dependent standard cell characteristic. However, Teene teaches: wherein said parasitic-dependent standard cell characteristic is selected from the group of standard cell characteristics consisting of: timing, power, input capacitance, noise, and any other parasitic-dependent standard cell characteristic (Col 10, lines 30-38, i.e. discussion of pre-layout timing and capacitance values of standard cell).

19. With respect to claims 15 and 31, Gupta teaches all the elements of claims 1 and 17, from which the claim depends respectively. Gupta teaches: at least one transformation comprises diffusion area and perimeter assigning of transistors of said standard cell, and adding wiring capacitances to said pre-layout representation (Col 4, lines 44-68, i.e. discussion of diffusion sharing and eliminating diffusion gaps). Gupta does not teach: wherein said characteristic comprises a parasitic-dependent timing characteristic of said standard cell. However, Teene teaches: wherein said characteristic comprises a parasitic-dependent timing characteristic of said standard cell (Col 10, lines 30-38, i.e. discussion of pre-layout timing/capacitance values of the standard cell component). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Teene into the invention of Gupta because Teene suggests that this pre-layout timing analysis can improve the invention of Gupta by quickly revealing gross timing violations, critical paths, for both worst-case and best-

case conditions, plus the effect of estimated power dissipation (see Col 8 line 65 - Col 9 line 4), all of which are critical elements well known in the art of circuit design.

Allowable Subject Matter

20. Claims 5, 10, 21 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

With respect to claims 5 and 21, the prior art made of record fails to teach all the inventive steps recited in claims 5 and 21. Specifically, the prior art made of record fails to teach: wherein a constructive estimator obtains said pre-layout estimation of said standard cell that is accurate to within about 1.5 percent of a post-layout timing characterization of a parasitic-dependent timing characteristic of said standard cell.

With respect to claims 10 and 26, the prior art made of record fails to teach all of the inventive steps of claims 10 and 26. Specifically, the prior art made of record fails to teach: w is estimated as Wc/2 + Spc in the instance a net associated with said diffusion region is an inter-MTS net.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suchin Parihar whose telephone number is 571-272-6210. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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